Low Complexity Architecture of N-Path Mixers for Low Power Application

A Al, T Taris, E Lauga-Larroze, F Podevin, S Subias, S Bourdel

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A. Al Shakoush
RFIC-Lab,
Univ. Grenoble Alpes
F-38031 Grenoble, France
ali.al-shakoush@univ-grenoble-alpes.fr

E. Lauga-Larroze
RFIC-Lab,
Univ. Grenoble Alpes
F-38031 Grenoble, France
estelle.lauga-larroze@univ-grenoble-alpes.fr

S. Subias
RFIC-Lab,
Univ. Grenoble Alpes
F-38031 Grenoble, France
serge.subias@univ-grenoble-alpes.fr

T. Taris
IMS, UMR 5818
CNRS, Université de Bordeaux
F-33405 Talence, France
thierry.taris@ims-bordeaux.fr

F. Podevin
RFIC-Lab,
Univ. Grenoble Alpes, Grenoble-INP
F-38031 Grenoble, France
florence.podevin@univ-grenoble-alpes.fr

S. Bourdel
RFIC-Lab,
Univ. Grenoble Alpes, Grenoble-INP
F-38031 Grenoble, France
sylvain.bourdel@univ-grenoble-alpes.fr

***Abstract* — The complexity of harmonic rejection N-path mixer based receivers is studied in this paper. A solution to improve harmonic rejection without increasing the complexity is presented and compared with conventional LNA-first receivers. This solution is based on π-delayed driving signals that enable a N-path mixer to present the same harmonic rejection than its 2N-path counterparts while reducing by 2 the frequency of operation and showing a reduced number of differential gain stages and switches. A 5-path mixer is thus proposed. It allows rejecting up to the 8th harmonic with only 3 differential gain stages whereas only the 6th harmonic would be rejected with conventional topologies having the same number of amplifier stages.**

Keywords—N-Patch mixer, mixer-first, receiver, software-defined radio, harmonic rejection, blocker

I. Introduction

With the development of Software Defined Radios (SDR) and the multi-standards dedicated to 5G, there is today a growing interest for wideband receivers. Receivers based on N-Path Mixers (NPMs) are good candidates since they are inherently wideband, tuneable and frequency selective. In addition, they are very attractive for low power and low cost systems. A major drawback of these structures is their sensitivity to blockers due to harmonics mixing. To reach large bandwidth receivers, harmonic rejection structures (HR-NPMs) have been proposed in [1], [2] and [3], leading to more complex systems. [1] and [2] present LNA-first receivers whereas [3] and [4] gives solutions for mixer-first receivers. While the latter achieves good linearity, LNA-first receivers provide good sensitivity. Whatever the considered structures, reducing the complexity of HR-NPMs is a major issue, specifically when wideband harmonic rejection is required.

In this context, this paper describes a low complexity and high harmonic rejection receiver, based on N-path mixers. The principle of harmonic rejection in NPMs is first detailed and a generic architecture representation for LNA-first receivers is given with a special focus on their level of intricacy. Then, their harmonic rejection performances are studied on the basis of the Effective Local Oscillator (EFLO) signal properties. In a second part, a structure based on π-delayed driving signals is presented and compared to other ones in terms of harmonic rejection and specific Figures-of-Merit related to complexity.

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II. Harmonic Rejection N-Path Mixers (HR-NPMs)

A. Principle

A simple NPM with N=4 (4PM), fed with an input signal $v_s(t)$, is depicted in Fig.1, on the basis of [4]. $v_s(t)$ is distributed over N paths that consist each in a switch and a capacitor. The switch is driven by a delayed version of the LO: $S_h(t)$, a periodic square signal with a duty cycle equal to $1/N$. The output of each path ($out_n(t)$) is a sampled version of the input signal and is expressed as follows:

$$out_n(t) = v_s(t).eflo(t) \tag{1}$$

where $eflo(t)$ is the Effective Local Oscillator (EFLO) signal that transposes the RF input.

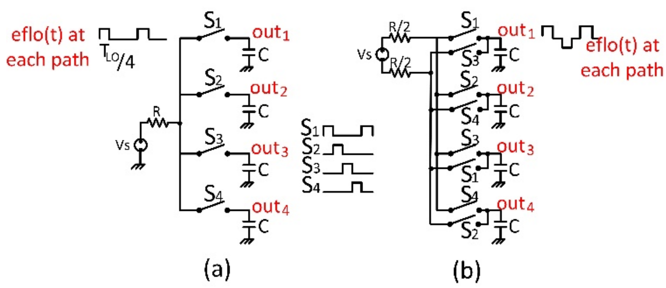


Fig. 1. The structure of a 4PM with (a) single, (b) differential modes.

This structure achieves a selective RF filtering that can be tuned accordingly to the LO frequency. Selectivity is proportional to N as explained in [5]. However, it suffers from a main issue that limits its applicability: the presence of harmonics in $eflo(t)$ generates harmonic mixing [6]. By using an RF differential signal as depicted on Fig. 1b, the even harmonics can be removed from the frequency spectrum of $eflo(t)$.

B. Generic Architecture of HR-NPMs

A generic topology is proposed in Fig. 2. This representation is well suited to LNA-first architectures. However strong similarities exist with mixer-first receivers. It consists of N paths and H branches. Along each path, H switches, driven by $S_h(t)$, sample the input RF signal through H gain stages (G_h). The computation of the gain coefficients has been studied in previous works with several methodologies [5]. In this work, we consider that *eflo(t)* is based on a sine wave sampled with a sampling frequency $F_s=H.F_{LO}$, which maximizes the number of null coefficients. Hence the complexity of the design is reduced as a null gain stage, $G_h=0$, does not need to be implemented. These coefficients are given by the following series defined for $0 \le h \le H\text{-}1$:

$$G_h = \sqrt{2}\sin\left(\frac{2\pi}{N}\left(1+h\frac{N}{H}\right)\right) \tag{2}$$

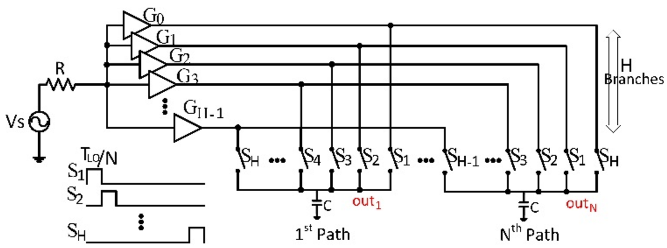


Fig. 2. *Generic topology of a HR-NMP*

Since *eflo(t)* is a sampled and hold sine wave, it can be expressed by means of G_h as follows:

$$eflo(t) = ol_s(t) * g(t) = \sum_{h=-\infty}^{\infty} G_h.\delta\left[t-\left(1+h\frac{N}{H}\right)T_s\right] * g(t) \tag{3}$$

where $ol_s(t)$ is the sampled version of the sine wave with sampling frequency $F_s=H.F_{LO}$ and *g(t)* is the square function of width $T_s=T_{LO}/N$.

Fig. 3 shows *eflo(t)* for the conventional NPMs of Fig. 1 obtained for H=1 and H=2 with N=4, respectively, whereas *eflo(t)* for the HR-8PMs, that will be further illustrated on Fig. 5, is obtained for H=8 and N=8. Increasing H leads to a better fit of *eflo(t)* with a pure sine wave.

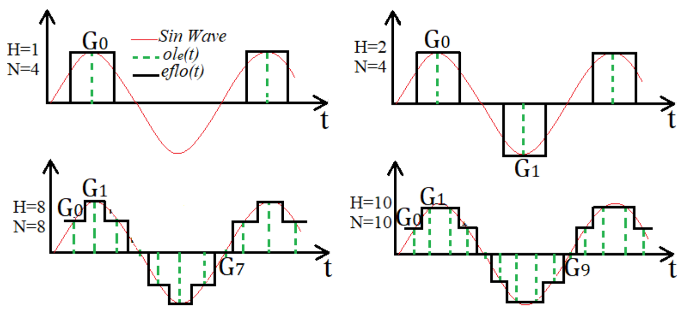


Fig. 3. Sampling coefficients of a sine wave for various H and N

The output signal (*outn(t)*) spectrum at each path is given by (4):

$$OUT_n(f) = V_S(f) * EFLO(f) \tag{4}$$

with:

$$\left|EFLO(f)\right| = \frac{A}{2}H.F_{LO}.T_s\text{sinc}(\pi T_s f)\sum_{n=0}^{+\infty}\delta(f-nH.F_{LO}\pm F_{LO}) \tag{5}$$

where A is the amplitude of *g(t)*.

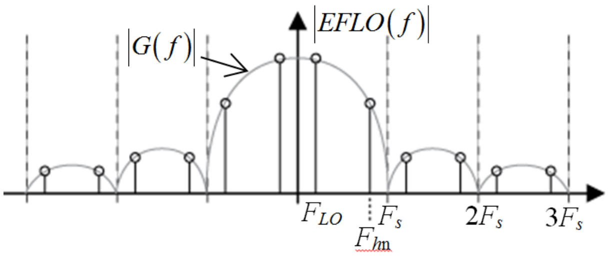


Fig. 4. Frequency response of the effective LO, *eflo(t)*.

As represented on Fig. 4, harmonics occur at $F_{hn}=n.F_s \pm F_{LO}$ that will be in the meantime the folded harmonics. Hence, the highest rejected harmonic is $H_r=(H\text{-}2)$ which is equal to 6 for the HR-8PMs of [1] and [2] where $H = N = 8$. In fact, many HR-NPMs have been proposed in the literature, for example in [1]-[4] but most of them are differential structures with eight paths, i.e. $N = 8$, while H, the number of samples per period, equals N, i.e. $H = N = 8$ as displayed on Fig. 5.

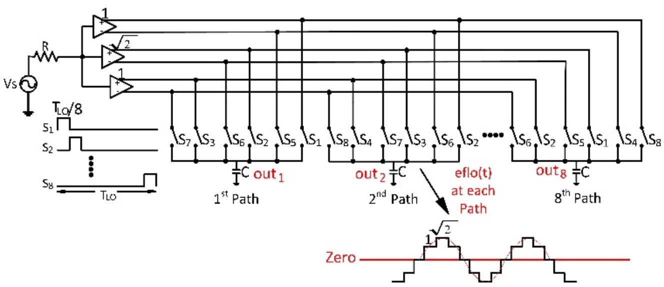


Fig. 5. Structure of a HR-8PM LNA-first receiver with a differential structure, as in [1] or [2]. Eight paths and eight samples. Samples corresponding to a null value do not need to be implemented theoretically.

The synthesis for HR-8PMs with 8 samples consists in splitting each path into 3 differential branches with specific gain ratios [1;√2;1], on the basis that 1/√2 corresponds to the sine of 45°, i.e. 1/8 of a sine period. Depending on the receiver architecture, the gains come from LNA in LNA-first receiver or from baseband amplifier in mixer-first topology. This allows the rejection of the 3rd and 5th harmonics during mixing. Hence the first harmonic that arises in the frequency spectrum of *eflo(t)* is $7F_{LO}$, the last one to be rejected is $6F_{LO}$.

C. *Complexity Analysis*

The performance in terms of harmonic rejection and selectivity are respectively related to H and N whereas the complexity is related to the number of gain stages, H_g, and the number of switches, S_w. Hence, ratios $\eta_1=H_r/H_g$ and $\eta_2=H_r/S_w$ are interesting Figures-of-Merit (*FoM*) in terms of harmonic rejection relatively to complexity.

As previously stated, in most cases, coefficient G_h is achieved through a gain stage. Conventionally, to reach the highest harmonic rejection as possible, H is equal to N, which results in a high number of gain stages. In other words, the system complexity increases with the targeted harmonic rejection. Fortunately, the effective number of branches, H_{ef}, corresponding to the number of branches to be physically implemented, is reduced when some coefficients G_h of *eflo(t)* are null as it is the case on Fig. 5 where $H_{ef} = 6$ while $H = 8$. This means that the number of gain stages, H_g, is equal to H_{ef}. In the case of RF differential input, the number of differential gain stages, H_g, is reduced to $H_{ef}/2$. In both cases, the total number of switches is $S_w = H_{ef}.N$.

For a given H (i.e. a given harmonic rejection $H_r = (H-2)$), the normalized coefficients G_h are described in Table 1, in which the number of coloured cells corresponds to H_{ef} while the number of dark coloured cells corresponds to the number of differential gain stages, H_g. The maximum rejected harmonic, H_r, the number of gain stages, H_g, and the number of switches, S_w, are reported in the column entitled ($H = N$) for conventional structures as previously reported. It appears that (i) even structures are favoured to odd ones, (ii) for some even numbers of paths, the sampling coefficients appear twice in half of a period, with a perfect symmetry. This corresponds to an integer number of non-null samples in a quarter of period, that is to say, the following cases: $H = 2(2i+1) = 6, 10, 14, 18, \ldots$ Those cases are particularly interesting in terms of coefficients symmetry. This symmetry can be leveraged to propose a very performing architecture based on π-delayed driving signals.

TABLE I. NORMALIZED COEFFICIENTS FOR A SINE PERIOD FOR VARIOUS SAMPLING OF THE SINE WAVE OF FREQUENCY F_{LO}.

	Conventionnal (H=N)																			Presented (H=2N)				
H	H_r	H_g	Sw	η_1	η_2	G_0	G_1	G_2	G_3	G_4	G_5	G_6	G_7	G_8	G_9	G_{10}	G_{11}	G_{12}	G_{13}	H_r	H_g	Sw	η_1	η_2
5	3	2	20	1.50	0.15	1.62	1	-1	-1.62	0														
6	4	2	24	2.00	0.17	1	1	0	-1	-1	0									4	1	6	4.00	0.67
7	5	3	42	1.67	0.12	1.82	2.26	1	-1	-2.26	-1.82	0												
8	6	3	48	2.00	0.13	1	1.41	1	0	-1	-1.41	-1	0											
9	7	4	72	1.75	0.10	2.67	4.09	3.59	1	-1	-3.59	-4.09	-2.67	0										
10	8	4	80	2.00	0.10	1	1.62	1.62	1	0	-1	-1.62	-1.62	-1	0					8	3	30	2.67	0.27
11	9	5	110	1.80	0.08	2.71	4.61	5.00	3.82	1	-1	-3.82	-5.00	-4.61	-2.71	0								
12	10	5	120	2.00	0.08	1	1.72	2.00	1.72	1	0	-1	-1.72	-2.00	-1.72	-1	0							
13	11	6	156	1.83	0.07	1.94	3.41	4.12	3.88	2.76	1	-1	-2.76	-3.88	-4.12	-3.41	-1.94	0						
14	12	6	168	2.00	0.07	1	1.82	2.26	2.26	1.82	1	0	-1	-1.82	-2.26	-2.26	-1.82	-1	0	12	5	70	2.40	0.17

III. N-PATH MIXERS BASED ON Π-DELAYED DRIVING SIGNALS

A. Principle

With conventional HR-NPMs, for which $H = N$, the large number of branches required to reach high rejection leads to high VCO frequency, related to the sampling frequency $F_s = H.F_{LO}$. As $H = N$, this also leads to numerous switches and to numerous amplifiers which just goes in disfavour of simplicity and power consumption. To increase harmonic rejection while keeping a low VCO frequency and without pushing up intricacy, a solution consists in choosing $H = 2N$ where $N = (2i+1)$ is an odd number of paths. The resulting HR-NPM presents only N paths and a smart combination of switches together with their driving signals enable to synthesize an effective local oscillator signal with $H = 2N$ samples. Practically, two versions of driving signals are used to control the switches: one for the positive branches, S_h^+, which generate a positive effective LO, $eflo^+(t)$, and one for the negative branches, S_h^-, which generate a negative effective LO, $eflo^-(t)$, as shown in Fig. 6. S_h^- is simply a π-delayed version of S_h^+. Combined with the appropriate gains G_h, the EFLO signal at each path is similar to the standard EFLO of a conventional HR-NPM where $H = N = 2(2i+1)$. It has to be mentioned that the VCO frequency needed for this π-delayed architecture is not equal to $2N.F_{LO}$ but only to $N.F_{LO}$ which is a great advantage for clock generation and distribution in the IC. Finally, the reduced number of paths, N, leads to lower complexity. As illustrated on Fig. 6, or in Table 1, with this solution, the number of differential gain stages is equal to half the number of non-null coefficients reduced by one, $H_g = (H_{ef}/2 - 1)$ The total number of switches is only $S_w = (H_{ef}/2 - 1).N$ in that case where $H_{ef} = H$-2.

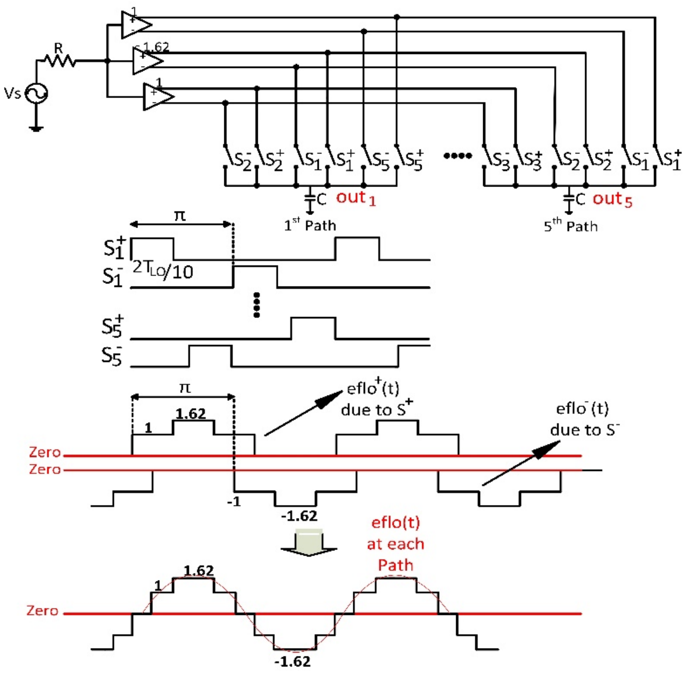


Fig. 6. π-delayed architecture with $H = 10$ and $N = 5$.

B. Simulation results

Frequency response of the presented N-path π-delayed structure has been carried out theoretically with Matlab software in order to validate the harmonic rejection in the case of $H = 10$ (and so $N = 5$) and to provide a comparison with conventional LNA-first topologies based on non-delayed structures [1]. Simulation results are illustrated Fig. 7. The first harmonic occurs at 3.6 GHz for an input frequency signal of 400 MHz which corresponds to the 9th harmonic. Simulations also confirm that the same harmonic rejection is reached with $H = N = 10$.

For $N = 5$ and $H = 10$, the presented solution needs to implement $H_g = 3$ differential LNAs and $S_w = 30$ switches whereas the equivalent $H = N = 10$ standard structure requires $H_g = 4$ LNAs and $S_w = 80$ switches. In addition, the frequency response of the π-delayed structure is compared to a standard HR-NPM which has quite a similar complexity ($H_g = 3$, $S_w = 48$) corresponding to $H = N = 8$. As expected the 7th harmonics occurs at 2.8 GHz reducing the system bandwidth as compared to the presented solution. Table 1 shows the Figures-of-Merit $\eta_1 = H_r/H_g$ and $\eta_2 = H_r/S_w$. They strongly go in favor of the π-delayed architecture.

In terms of theoretical sensitivity, Fig. 8 shows the effects of the gain ratio error and the phase error between the output LNAs signals, of respective gains 1 and 1.62, on the fundamental response of the effective LO, *eflo(t)*, over its harmonic response. This ratio, *HR-Fun/har*, is proportional to the HRR of the total mixer. It is observed from the curves that the system performance decreases when increasing the mismatching between the output LNA signals. The slope of *HR-Fun/har* with respect to the gain error is faster than the slope with respect to the phase error, which concludes that our system is more sensitive to LNA gain error than phase error. LNA errors can be potentially overcome thanks to biasing adjustment. There cannot be observable *HR-Fun/har* due to LNA on the 5th harmonic since the clock duty cycle is equal to 1/5.

In comparison to the state of the art, our theoretical study of the proposed structure shows an improvement on the 5th harmonic rejection with respect to the gain and phase LNA outputs mismatching. Furthermore, it can be outlined using equations of harmonic attenuation (HA) [7], that the 3rd HA of our proposed architecture shows similar behavior with the conventional HR8PM. This results depends on the gain and phase errors between the output LNA signals.

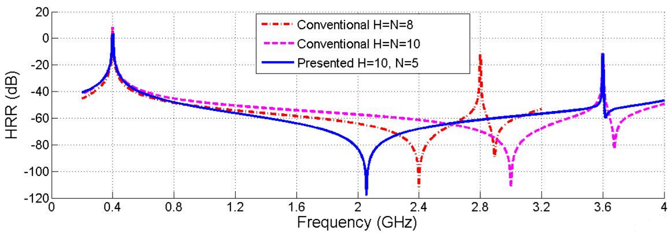
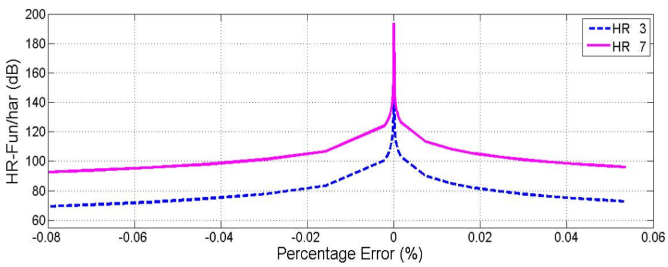
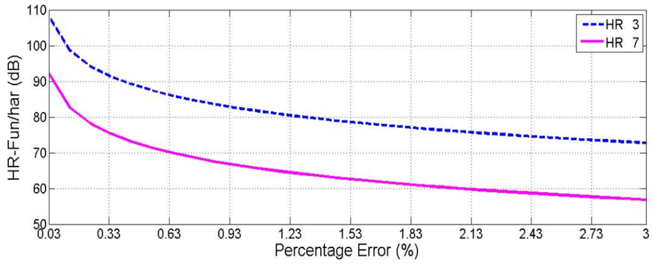


Fig. 7. Matlab simulations of the presented solution based on π-delayed driving signals for $H = 10$ and $N = 5$ (solid line). Comparison with conventional structures with $H = N = 8$ (light dashed line) and $H = N = 10$ (dark dashed line).



(a) Gain ratio error



(b) Phase error

Fig. 8. Matlab simulations showing the effect of (a) the gain ratio error on the HR-Fun/har of the eflo(t) of the proposed architecture with zero phase error and (b) the phase error between output LNA signals on the HRR of the eflo(t) of the proposed architecture with zero gain error. No impact is observed on HR-Fun/har for 5th harmonic.

IV. Conclusion

A theoretical, general, study has been proposed that can be useful for the design of conventional N-path mixers based on LNA-first receivers. This approach highlights some particular cases of odd numbers of paths presenting interesting symmetrical properties in terms of sampling gain coefficients. This symmetry has been utilized in the framework of a π-delayed driving signals architecture that enables high harmonic rejection while using a lower VCO frequency and presenting a lower complexity, in terms of the required number of differential amplifiers and switches, than its conventional counterparts. The solution is illustrated by a 5-path mixer that achieves a high harmonic rejection up to the 8th harmonic with only 3 differential amplifiers and 30 switches.

Acknowledgment

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References

[1] Y. Xu, J. Zhu, P. R. Kinget, "A Blocker-Tolerant RF Front End With Harmonic-Rejecting N-Path Filter", *IEEE Journal of Solid-State Circuits*, vol.53, no.2, pp.327–339, 2018.

[2] Z. Ru, N. A. Moseley, E. A. M. Klumperink, B. Nauta "Digitally Enhanced Software-Defined Radio Receiver Robust to Out-of-Band Interference", *IEEE Journal of Solid-State Circuits*, vol.44, no.12, pp.3359–3375, 2009.

[3] C. Andrews, A. C. Molnar "A Passive Mixer-First Receiver With Digitally Controlled and Widely Tunable RF Interface", *IEEE Journal of Solid-State Circuits*, vol.45, no.12, pp.2696–2708, 2010.

[4] C. Andrews, A. C. Molnar "Implications of Passive Mixer Transparency for Impedance Matching and Noise Figure in Passive Mixer-First Receivers", *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol.57, no.12, pp.3092–3103, 2010.

[5] E. A. M. Klumperink, H. J. Westerveld, B. Nauta, "N-Path Filters and Mixer-First Receivers: A review", *Proc. IEEE Custom Integrated Circuits Conf. (CICC)*, pp.1–8, 2017.

[6] C. Andrews, C. Lee, A. Molnar, "Effects of LO Harmonics and Overlap Shunting on N-Phase Passive Mixer Based Receivers", *Proc. ESSCIRC (ESSCIRC) 2012*, pp.117–120, 2012.

[7] Y. Xu, J. Zhu, P. Kinget, "A Blocker-Tolerant RF Front End With Harmonic-Rejection *N*-Path Filter", *IEEE Journal of Solid-State Circuits*, vol.53, no.2, pp.327–339, 2018.